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What Is Claimed Is:

1. A semiconductor device, comprising:

a substrate;

a plurality of gate electrodes having offset nitride films and side wall spacers for forming contact holes in a self-aligning fashion, provided on said substrate via a gate insulation film;

an interlayer insulation film that covers said gate electrodes; and

contact holes that go through said interlayer insulation film between a plurality of said gate electrodes,

wherein the said wall spacers are constituted from lower side wall spacers that include a silicon oxide film and are provided on the lower sides of the gate electrode side walls, and upper side wall spacers that include a silicon nitride film and are provided on the upper sides of the gate electrode side walls.

2. A semiconductor device according to Claim 1,

wherein said lower side wall spacers are provided in a state of contact with the lower sides of said gate electrode side walls, and said upper side wall spacers in a state of contact with the upper sides of said gate electrode side walls.

3. A semiconductor device according to Claim 1,

wherein said lower side wall spacers are thick enough at the interface between the silicon oxide film forming said lower side wall spacer and the silicon nitride film forming said upper side wall spacer to make the distance between said

interface and said substrate such that no hot carrier phenomenon will occur.

4. A semiconductor device according to Claim 1,

wherein a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered are formed on said substrate, and

the film thickness of said lower side wall spacers in said dense region are greater than the film thickness of said lower side wall spacers in said sparse region.

5. A semiconductor device comprising:

a substrate; and

gate electrodes having side wall spacers, provided on said substrate,

wherein said side wall spacers comprise lower side wall spacers that are composed of a silicon oxide film and are provided on the lower sides of the gate electrode side walls, and upper side wall spacers that are composed of a silicon nitride film and are provided on the upper sides of the gate electrode side walls.

6. A semiconductor device according to Claim 5,

wherein said lower side wall spacers are provided in a state of contact with said lower sides of said gate electrode side walls, and said upper side wall spacers in a state of contact with the upper sides of said gate electrode side walls.

7. A semiconductor device according to Claim 5,

wherein said lower side wall spacers are thick enough at the interface between the silicon oxide film forming said lower side wall spacer and the silicon nitride film forming said upper side wall spacer to make the distance between said interface and said substrate such that no hot carrier phenomenon will occur.

8. A semiconductor device according to Claim 5,

wherein a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered are formed on said substrate, and

the film thickness of said lower side wall spacers in said dense region are greater than the film thickness of said lower side wall spacers in said sparse region.

9. A method for manufacturing a semiconductor device, comprising:

a first step of forming on a substrate a plurality of gate electrodes having offset nitride films and gate insulation films;

a second step of forming a silicon oxide layer including a silicon oxide film so as to cover said substrate and said gate electrodes;

a third step of forming a lower side wall spacer precursor layer that is thinner than said gate electrodes by etching said silicon oxide layer;

a fourth step of forming a silicon nitride layer including a silicon nitride film so as to cover said lower side wall spacer precursor layer;

a fifth step of successively etching said silicon nitride layer and said lower side wall spacer precursor layer and thereby forming side wall spacers having a structure consisting of an upper side wall spacer in which a silicon nitride film remains on the upper side of the side wall, and a lower side wall spacer in which a silicon oxide film remains on the lower side of the side wall;

a sixth step of forming an interlayer insulation film so as to cover said gate electrodes where side wall spacers have been formed; and

a seventh step of etching the interlayer insulation film and thereby self-aligningly forming contact holes that go through said interlayer insulation film.

10. A method for manufacturing a semiconductor device according to Claim 9,

wherein, in said first step, a plurality of said gate electrodes are formed so as to constitute a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered, and

when this results in the film thickness in said dense region of said silicon oxide layer formed in said second step being greater than the film thickness in said sparse region,

a CMP step, in which said silicon oxide layer is smoothed out over a wide area by chemical machine-polishing, is performed ahead of said third step.

11. A method for manufacturing a semiconductor device according to Claim 9,

wherein, in said first step, a plurality of said gate electrodes are formed so as to constitute a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered,

during the formation of said silicon oxide layer in said second step, the film formation material or film formation conditions is or are set so that the space between said gate electrodes in said dense region will be filled in and the film thickness on said upper side of said gate electrodes in said sparse region will be greater than the film thickness at said gate electrode side walls of said sparse region, and

in the third step, said lower side wall spacer precursor layer is formed by etching said silicon oxide layer so that the film thickness at said gate electrode side walls of said dense region is greater than the film thickness at said gate electrode side walls of said sparse region.

12. A method for manufacturing a semiconductor device according to Claim 11,

wherein said silicon oxide layer is formed using PSG, BPSG, P-TEOS · NSG, or P-$SiH_4$ · NSG.

13. A method for manufacturing a semiconductor device according to Claim 12,

wherein, after said second step, the third step is performed without smoothing said silicon oxide layer formed using PSG, BPSG, P-TEOS · NSG, or P-$SiH_4$ · NSG.

14. A method for manufacturing a semiconductor device according to Claim 11,

wherein the film thickness distribution of said silicon oxide layer is such that the film is thick enough in said dense region that there are no steps on said silicon oxide layer surface caused by said gate electrodes, and the film is thin enough in said sparse region that steps caused by said gate electrodes remain on said silicon oxide layer surface.